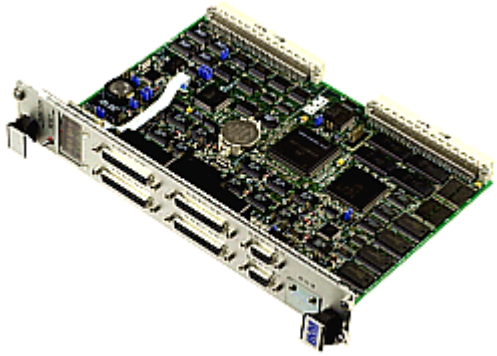
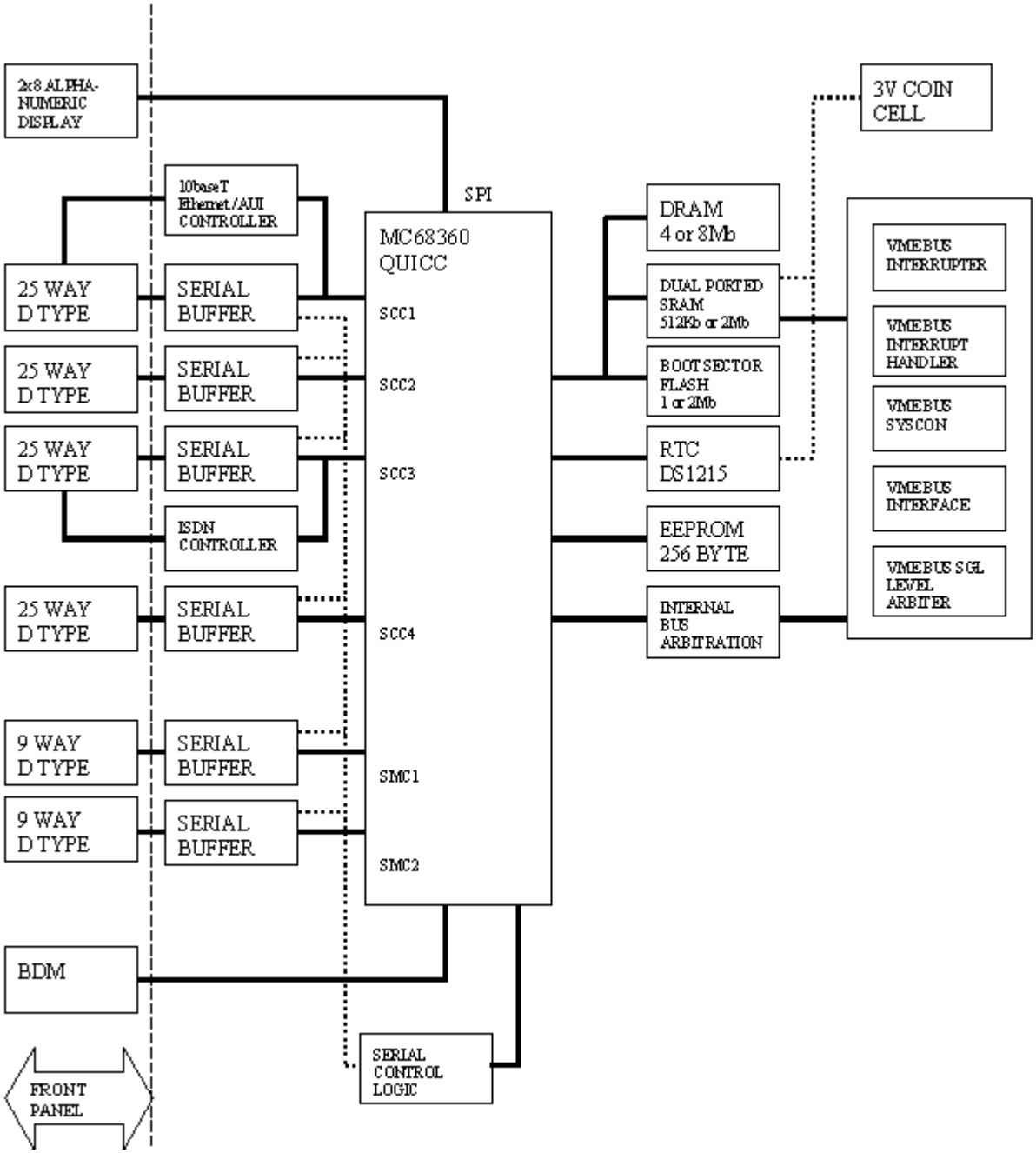
BVME3100 68360 VMEbus Communications Controller

The BVME3100, is an Intelligent VMEbus Serial Controller based on the 68360 CPU at 32MHz. Ample memory space is provided with 2Mb BOOTFLASH, 2Mb SRAM, and 8Mb DRAM. Six serial channels are available one with an Ethernet option and one with an ISDN option. Line termination can be selected as RS232, RS422 or RS485. A special feature is the 16 character alphanumeric display on front panel which can be used for user messages or line status indication under software control. A VMEbus Master/Slave Interface is also included enabling the BVME3100 to be used in a variety of applications.



Key Features

- MC68360/MC68EN360/MC68MH360 processor at 32MHz.
- 4 or 8Mbytes of 32-bit wide DRAM.
- 1 or 2Mbyte of 16-bit wide BOOTFLASH PROM (4 x 8-bit wide AM29F040).
- 512k or 2Mbytes of 32-bit non-volatile (battery backed) SRAM.
- 256 byte EEPROM for configuration settings.
- A24/D16 Master/Slave VMEbus Interface.
    - VMEbus Interrupter.
    - VMEbus Interrupt handler.
    - Location monitor - Mailbox Interrupt.
    - Single Level Arbiter.
    - RESET, SYSCLK generator, Bus Timeout BERR generator.
- Battery backed Real Time Clock.
- Reset/Function (Abort) toggle switch.
- 16 Character Alphanumeric display on the SPI bus.
- EMI Screened display window.
- BDM Interface available on front panel.
- SCC1 Port provides RS232/422/485 or Ethernet.
    - SCC1 mode selection under software control.
    - SCC1 10baseT/AUI Ethernet mode selectable via links.
- SCC3 Port provides RS232/422/485 or ISDN.
    - SCC3 mode selection under software control.
- SCC2 and SCC4 ports provide RS232/422/485 serial interface.
    - SCC2 and SCC4 mode selection under software control.
- SMC1 and SMC2 RS232 serial ports.
- SCC1, SCC2, SCC3 and SCC4 available via front panel 25 way "D" sockets.
- SMC1 and SMC2 available via front panel 9 way "D" sockets.
- EMC Compliant 8HP front panel.
- BVME3000 architecture compatible.
- OS-9 software support.



Processor

The BVME3100 is based on the MC68360 32-bit Quad Integrated Communications Processor from Motorola running at 32MHz. The 68360 provides a number of I/O functions including 4 Serial Communication Controllers, 2 SMC Transparent Serial ports, counter timers, general purpose I/O and an SPI port.

The 68EN360 supports the Ethernet protocol which can be operated via SCC1 of the BVME3100. The 68MH360 supports the ISDN protocol which can be operated via SCC3 on the BVME3100.

All of the 68360's provide a BDM and JTAG test facility for module debug.

Memory

The BVME3100 can be supplied with FLASH, SRAM, DRAM and EEPROM memory in various build options.

FLASH Memory

The BVME3100 can be built with 1 or 2Mbytes FLASH in 1Mbyte banks, implemented using 2 AMD Am29F040 (or compatible) 70ns devices (512k x 8) per bank. The FLASH memory is 16-bits wide but may be read as 8, 16 or 32-bits wide due to the auto bus sizing features of the 68360 processors.

Writing to FLASH is supported at 8, 16 and 32-bits wide. The manufacturers recommended programming algorithm is for 8 bit writes only.

The BVME3100 is designed to boot directly out of FLASH once the memory has been programmed. The boot FLASH must be programmed via the BDM interface before the BVME3100 can boot. This would be the normal operating mode. The bottom 128kbytes of FLASH memory may be write protected by installing a link DRAM Memory

The BVME3100 can be built with 4 or 8Mbytes of DRAM in 4Mbyte banks, implemented using 2 Hitachi HM5118160 70ns devices (1M x 16) per bank. The DRAM is 32-bits wide and supports 32-bit fast page mode access. The DRAM may also be accessed as 8, 16 or 32-bits wide due to the auto bus sizing features of the 68360 processors. The 68360 performs DRAM refreshing, 1024 cycles in 16ms and DRAM address multiplexing.

SRAM Memory

The BVME3100 can be built with 512kbyte or 2Mbytes of SRAM, implemented using either 4 off 68128 70ns devices (128k x 8) for 512kbytes SRAM or 4 off 628512 70ns devices (512k x 8) for 2Mbytes of SRAM. The SRAM is 32-bits wide and may be accessed as 8, 16 or 32-bit memory due to the auto bus sizing features of the 68360 processors. Low power version of the SRAM chips are used in order to maximise the memory storage capacitor/battery life.

In the absence of the +5V supply the SRAM is normally backed up by the on-board memory capacitor for 10 days typically when fully charged. If the P1 standby pin is connected then this will be used when the capacitor is discharged. For a longer SRAM on-board backup, the real time clock battery may be used to backup the SRAM when link selected, giving a backup life of about 10 years typically (including the real time clock supply).

EEPROM Memory

The BVME3100 is fitted with a 256byte EEPROM (Xicor 25020) controlled over the master 68360 SPI bus. The part can be programmed to be block protected in ¼ or ½ device size blocks. A link may be installed to fully write protect the EEPROM

Real Time Clock

The BVME3100 provides a battery backed real time clock shadowed under the even byte of the lower 1Mbyte of the FLASH memory. The clock provides full date and time functions, and is battery backed using a lithium battery giving typically 10 years of non-volatile operation.

Serial Ports

The BVME3100 has 4x25-way D-type serial ports and 2x9-way D-type serial ports located on the front edge of the board. The serial ports use LTC1321 transceivers, which may be RS232, RS422 or RS484 depending on the software selection. RS232 asynchronous baud rates of up to 115.2Kbits/s are supported, this restriction is due to the RS232 serial buffer devices and is not a limitation of the 68360. Similar restrictions apply to RS422 and RS485.

Ethernet Port

SCC1 on the BVME3100 may be used to provide a 10baseT (twisted-pair) Ethernet port for a 68EN360 version of the board. An external 25-way D-type to RJ45 adapter is used, but all of the 10baseT circuitry is on-board.

ISDN Port

SCC3 on the BVME3100 may be used to provide an ISDN port for the 68MH360 version of the board. An external 25-way D-type to RJ45 adapter is used, but all of the ISDN circuitry is on-board.

Local Bus Monitor/Watchdog

Local Bus monitoring on the BVME3100 is controlled by the 68360. A programmable register in the 68360's DPR must be set to enable BERR and to derive the timeout period. This function is necessary to prevent CPU hang-up as a result of invalid addresses being generated.

The watchdog monitor on the BVME3100 is controlled by the 68360. A programmable register in the 68360's DPR must be set to enable the watchdog. The register can only be programmed once after reset, and initialises when the watchdog is enabled.

Reset/Function (Abort) Switch

The BVME3100 is fitted with a bi-directional toggle switch. Pushing the switch away from the board will generate a reset (if link selected) and pushing the switch towards the board will generate an abort (if link selected), causing an auto-vectored level 7 interrupt to be generated to the 68360, or can be detected in a register if used for "function".

Power Supply Monitor/Reset

A MAX791 provides power up/power down control for the non volatile RAM and Processor Reset. The Processor can generate an SRESET signal if a software reset occurs, which is driven into the MAX791 to generate a full system reset if link selected.

ACFAIL

A VMEbus compatible ACFAIL signal from the P1 connector may be used to generate an auto-vectored level 7 interrupt to the 68360 (if link selected).

LED Indicator

Three on-board GREEN-LED's indicate that +5V, +12V and -12V power is applied to the board. See section "Figure 3 Board Layout (Excluding Front Panel) (page)" for the position of these indicators.

Interrupts

VMEbus Interrupt Handler

The BVME3100 will support VMEbus interrupts on all 7 levels. A board control register can be programmed to enable each IRQ level individually.

A user vector VMEbus interrupt causes the CPU to reply with a VMEbus Master Interrupt acknowledge cycle. This cycle uses only IACK that is broadcast in a similar way to the addresses. The A1, A2 and A3 address lines indicate the address level being handled.

The interrupting device returns an ID vector on the odd data byte. This is used as the user vector by the CPU.

Internal Interrupts

Internal CPU interrupts are generated from a variety of sources, as detailed in the table below:

Level	Source	Type
7	VME IRQ7 Abort switch ACFAIL	Vectored Autovectored Autovectored
6	VME IRQ6 ISDN IRQ	Vectored Vectored
5	VME IRQ5	Vectored
4	VME IRQ4	Vectored
3	VME IRQ3	Vectored

2	VME IRQ2 Location Monitor	Vectored Autovectored
1	VME IRQ1 ISDN IRQ	Vectored Vectored
Internal	Variable (see following paragraph)	

The ISDN interrupt is generated on either level 1 or level 6. A board control register is used to select the interrupt level.

The 68360 can also generate internal interrupts to control the operation of its internal peripherals. Although an external cycle does not occur the interrupts will effect the priority of the external interrupts and thought must be given to the internal interrupt levels. The 68360 has three main sources of Internal Interrupts:-

The CPM which controls the SCC's, parallel I/O, timers, DMA, SPI and the RISC timer table.
The PIT, which is an internal timer derived from the SPI clock.
The SWT which is the software watchdog timer.
The CPM and PIT can be programmed to generate an interrupt on any level while the SWT can only generate an Interrupt on level 7 if selected.
The CPM interrupt sources all share the same interrupt, however these can be prioritised inside the CPM.

VMEbus Interrupter

The BVME3100 can generate VMEbus interrupts on any programmable single level 1- 7 and responds with a software programmable ID to the subsequent interrupt acknowledge cycle. Writing the ID to the vector register causes a VMEbus interrupt to be generated on the selected level. The BVME3100 VMEbus interrupt ID vector may be programmed to suit the application.

VMEbus Interface

VMEbus Master
Byte or word Master accesses may be made to the standard (A24) and short (A16) address spaces. Read Modify Write (RMW) cycles are supported.

The BVME3100 supports the Release On Request (ROR) VMEbus arbitration method. The method uses FAIR requesting, ensuring each master has an equal chance of obtaining the bus. Digital bus busy filtering and arbitration interleaving is used to ensure premium arbitration performance.

VMEbus Slave
The on-board SRAM on the BVME3100 is dual ported onto the VMEbus. The VMEbus base address is programmed into the board control register which can be set on 512Kbyte boundaries anywhere in the (A24) address space. The BVME3100 supports byte, word and RMW cycles and is compatible with VMEbus address pipelining.

The BVME3100 provides a Location Monitor Interrupt which is set by an external Bus Master accessing standard A24 space at either 512Kbytes above the SRAM if it is on a 1Mbyte boundary (A19 clear in the board control register), or by accessing the SRAM if it is on a 512Kbyte boundary (A19 set in the board control register).

VMEbus System Controller Functions

The BVME3100 provides a number of system controller functions that may be enabled as follows:-

RESET
Asserted if the +5V falls below +4.7V when link selected. VMEbus RESET has a minimum asserted period of 200mS.

Arbitration
The BVME3100 is configured to support Single level arbitration when enabled in a board control register.

SYSCLK
The BVME3100 provides a 16MHz VMEbus SYSCLK when link selected.

VMEBERR
The BVME3100 provides a 128μ S Bus Timeout BERR signal when link selected.

The processor Bus Timeout BERR is 32μ S signal and is not linked to the VMEBus Timeout BERR. Therefore when doing a VMEbus master access, if an internal timeout occurs, the user should not perform another VME master access for 96μ S as the cycle cannot be guaranteed.

Front Panel Display

The display is an HCMS-2923 CMOS green LED alpha-numeric display providing 2 rows of 8 characters in a 5x7 dot matrix. This device incorporates the dot matrix LED's and display driver/decoder into a single package and is driven from the 68360 by serial data on the SPI bus.

Specification

ON-BOARD FUNCTIONS	
MC68360 or	Quad Integrated Communications Controller.
MC68EN360 or	Quad Integrated Communications Controller with Ethernet support
MC68MH360	Quad Integrated Communications Controller with ISDN support.
Serial Ports	32MHz with Background Debug Mode support. 6 off serial ports, software selectable between RS232/RS422/RS485. Connection via front panel 25-way & 9-way D-type connectors.
Network	1 serial port selectable for Ethernet, one serial port selectable for ISDN.
FLASH	1 or 2Mbyte (factory fitted), 16-bit wide, Bottom 128kbytes Boot protected.
SRAM	512kbytes or 2Mbytes CMOS SRAM, 32-bit wide, non-volatile for up to 10 years
DRAM	4 or 8Mbytes (factory fitted) 32-bit wide.
EEPROM	X25020 256 x 8 bit non volatile storage, accessed via SPI on the 68360.
Clock	DS1315S Timer Clock Peripheral Battery Backed for 10 years.
Display	HCMS-2923 2 row 8 character front panel display.
Battery backup	CR2450 500mAh lithium coin cell and memory capacitor
LOCAL BUS TIMEOUT	period 1024 CPU clocks (32m S @ 32MHz bus clock).
Indicators and switches	LEDs 3 green on board - for power indication. RESET/ABORT front panel switch, individual enable links.
Interrupts	Abort = level 7 auto-vectored interrupt. ACFAIL level 7 auto-vectored interrupt within 256m S.In
User Links	SRAM battery backup supply; RESET switch enable; ABORT switch enable; EEPROM write protect; FLASH boot block write protect; Ethernet mode; Serial termination
Program Links	EEPROM chip select; SERIAL mode select; AUTO-VECTORED level 7 source.
VMEbus System Controller Functions	
ARBITER	SGL, level3, FAIR ROR
SYSCLK	Driver
SYSRESET	Driver/Monitor power-up and switch
VMEbus RESET	minimum period = 200mS
BUS TIMEOUT	period 128m S
ACFAIL	(level 7 auto-vectored interrupt).