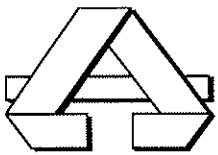
ACTIS Computer

IP module
Fast Ethernet™ Controller:
LAN-100
& LN-100

User's Guide

9747



ACTIS

COMPUTER S.A.

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ACTIS Computer S.A.
19 Chemin du Champ-des-Filles
1228 Plan-Les-Ouates / Geneva
Switzerland
Tel: +41 22-794 43 35 Fax: +41 22-794 43 91
Email : info@actis.ch Web : http://www.actis.ch

1. Overview

The LAN-100 IP module of ACTIS Computer is a Fast Ethernet controller compatible with the IP specification, able to operate at the 100 Mbps "fast Ethernet" speed as well as at 10 Mbps. It provides a standardised media-independent interface according to the IEEE 802.3u-1995 specification and is normally used in conjunction with the LN-100 twisted pair interface adaptor from ACTIS, for the 100BASE-TX as well as 10BASE-T connections on twisted-pair cables.

The LAN-100 may be operated on base-boards providing either 32 MHz or 8 MHz clock drive, although the higher frequency is recommended. A local memory buffer of 128 kbytes is provided for storage of transmitted and received packets. The adaptor architecture permits very high performance to be achieved from the hardware and software.

2. Summary of features

- Single-size IP module.
- 32 MHz capability as well as 8 MHz.
- Compatible with the VITA-4 specification.
- Supports IEE 802.3/ Ethernet™ network protocols at 10 Mbps and at 100 Mbps speeds (IEEE 802.3u)
- SMC "Feast" 91C100 Fast Ethernet controller
- 128 kbyte buffer memory with very efficient management by the controller.
- Standard MII interface to the 100 Mbps physical layer, plus 10BASE-T signals at 10 Mbps.
- 48-bit MAC address in local E^2PROM, automatically loaded into 91C100 registers as default address.
- Full-duplex operation supported.
- Physical-layer adaptor for 10BASE-T and 100BASE-TX options - on Category 5 twisted pair - available.
- Fibre-optic 100BASE-FX or other adaptors on request.

3. Description

The LAN-100 IP module contains an SMC 91C100 Feast™ controller, able to support the Fast Ethernet protocols at 100 Mbps to IEEE specification 802.3u-1995. It also supports 10 Mbps operation over twisted pair adaptors. The 91C100 is a very advanced device able to handle the CSMA/CD protocols for reception and transmission coupled with management of buffers in the local memory (128 kbytes of 20ns SRAM) to give a very high performance with comparatively simple, and therefore fast, software in the host.

The module contains no physical-layer transceiver devices. It provides an interface in compliance with the standard IEEE 802.3u for a "Media-Independent Interface" and can therefore be easily connected to a variety of external adaptors for 100 Mbps operation. The MII is defined for a 40-pin connector, and the IP connector has 50 pins, so the free pins have been employed to support an external 10 Mbps transceiver. The pin-out has been arranged to facilitate cabling to the standard MII 40-pin connectors if required. A physical-layer adaptor, combining a 100 Mbps transceiver to the 100BASE-TX standard with a 10 Mbps transceiver to the 10BASE-T standard is available from ACTIS Computer, reference LN-100.

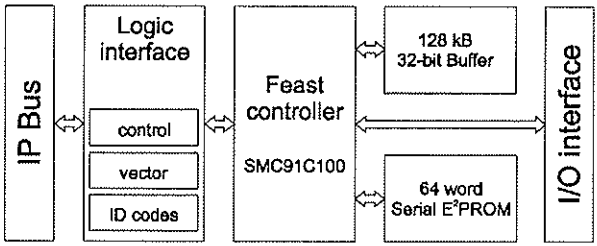
The IP interface is able to operate at either 32 MHz or 8 MHz clock frequencies. An interrupt vector register is included, and DMA functions supported for data transfer under host system control. Byte swapping is provided, under software control, for I/O and for DMA access to the data registers.

The standard 12-byte ID facility is included, so that the module type and other parameters may be examined by the host software. The 48-bit MAC address is stored in a small non-volatile memory and loaded automatically into the registers of the 91C100 when it is reset or on power-up.

3.1. Block diagram

The hardware architecture of the LAN-100 is divided into three main sections:

- The IP bus interface, controlling the timing at 8 MHz and at 32 MHz, with an interrupt vector register, control registers and an implementation of the ID ROM.
- The SMC 91C100 controller.
- The local 32-bit buffer memory of 20ns SRAM, providing 128 kbytes of storage for packets.
- The 64-word 16-bit E^2PROM holding the address.



3.2. LAN-100 characteristics

Symbol	Parameters	Min	Typ	Max	Unit
I_{cc}	Vcc supply current	---	180	280	mA
I_{ccPHY}	Drive current to LN-100	---	200	500	mA
T_a	Operating ambient temperature	0	---	+70	°C
T_{stg}	Storage temperature	-55	---	+150	°C
F_{MII}	MII clock output	24.998	25.000	25.002	MHz

3.3. IP address spaces

The following table defines the IP address spaces:

MEM space	Not Used
Identification space	12 bytes
I/O space	91C100 controller, plus other registers.
DMA access	Forces data register R/W
Interrupt ACK	Interrupt vector

The base addresses of the spaces will depend on the IP carrier.

3.4. I/O address space

The internal registers of the 91C100 "Feast" controller are mapped into the I/O space and cover a block of eight 16-bit words (16 bytes). They are arranged in four banks, as described below in detail. The registers are accessed using offsets $00 to $0E or $10 to $1E (16-bits access assumed): the difference is that in block $0x the data words correspond to those in the 91C1200 data sheets, whereas if block $1x is accessed the two bytes are interchanged. This feature will be useful in implementing drivers for various types of processor, when accessing the data FIFO registers.

There are three 8-bit control registers, at offsets $21, $23 and $25 (i.e. LSB byte) for the interrupt vector, a speed optimisation command, and a DMA control register.

I/O space address:	Bank	MS Byte register	LS Byte register
REGISTERS IN THE SMC 91C100			
$0E	All	Read-only $33	Bank number R/W
$00	0	TCR Transmission control register	
$02	0	EPH status register (last tx frame)	
$04	0	RCR Receive control register	
$06	0	Counters of collisions etc.	
$08	0	Memory info (read-only) $FF	
$0A	0	$35 read-only	Reserve tx mem.
$0C	0	Reserved register (read-only)	$00
$00	1	CR Configuration	IRQ enable
$02	1	Base address $1800: do not alter this	
$04	1	Individual address registers 6 bytes	
$06 $08	1 1	loaded automatically from E2ROM with organisationally unique ID + serial no.	
$0A	1	GP register R/W - used for E^2ROM data.	
$0C	1	CTR Control register, various functions	
$00	2	MMU Command reg. For buffer allocation and freeing, also Tx. commands made here	
$02	2	PNR Tx. Packet No.	ARR Allocated number
$04	2	FIFO: Rx. Pkt. No. Tx. done Pkt. No.	
$06	2	PTR Pointer register, buffer access mode	
$08	2	Data register: read Rx. Area or write to	
$0A		Tx. area - 4 bytes to permit 32-bit ops	
$0C	2	Interrupt status, enable, acknowledge.	
$00 to $07	3	64-bit multicast filtering table	
$08	3	MII management interface for PHY layer	
$0A	3	Revision register (Read) $3370 upwards	
$0C	3	ERCV early receive control register	
$10 to $1F		As above but LSB and MSB bytes are interchanged.	
OTHER REGISTERS (LSB byte only)			
$21		Interrupt vector register	
$23		Bus optimise: write $08 in 8 MHz systems	
$25		DMA Control register: 2 bytes write-only d2 swap bytes, d0 set DMA request.	

3.5. Identification address space

ID space addr.	Description	Value
$01	Ascii 'I'	$49
$03	Ascii 'P'	$50
$05	Ascii 'A'	$41
$07	Ascii 'H'	$48
$09	Manufacturer identification	$99
$0B	Module type	$35
$0D	Revision code	(Typically) $5F
$0F	Reserved byte	$00
$11	Driver ID, if used: Low byte	$00
$13	High byte	$00
$15	Number of bytes used	$0C
$17	CRC	(Typically) $4C

The first four bytes contain the ASCII text "IPAH" which identifies the start of the ID area and specifies 32 MHz capability. The manufacturer code defines ACTIS Computer s.a. as the maker, and the type code of $35 specifies that the IP is of type LAN-100.

The revision code is set to the ASCII constant for a space ($5F) at first, and to codes for 'A', 'B'... etc. thereafter.

Bytes at offsets $11 and $13 could be used for identification of a software driver, but are normally unused. The CRC is as described in the IP standards, and is the lower 8 bits of the F.C.S. as described in recommendation T.30 (Fascicle VII.3) of the ITU(T) (ex. C.C.I.T.T.).

Note that the ID "ROM" is in fact coded into a programmable logic device in the IP bus interface area, and that it can not be modified by the user. Special versions, for example with driver ID bytes, could be supplied by ACTIS if necessary as the design of the CPLD permits data to be altered.

3.6. Wait state cycles

The following table gives the number of wait states asserted in various conditions: these are the same for all types of address space including DMA access.

IP Clock	Conditions	Wait state R/W cycles
32 MHz	1 or more idle states	2
32 MHz	No idle states	3
8 MHz	After reset	As above
8 MHz	Write $08 to bus opt.	0

The maximum speed of access at 32 MHz is one 16-bit access per 5 bus clock periods, i.e. 156.25 ns, giving 12.8 Mbytes per second. The sequence of bus states at the limit is either:

Idle	select	wait	wait	terminate	idle	select	...

or

Idle	select	wait	wait	terminate	select	...

At 8 MHz the timing should be modified by writing $08 to offset $23. There will then be no wait states, and a data throughput of 8 Mbytes per second will be attainable. If the timing is not set to high speed at 8 MHz then only 3.2 Mbytes per second can be attained. The interface design permits the carrier board to assert "hold" states at 8 MHz.

It should be observed that the maximum throughput over the 100 Mbps "Fast Ethernet" is unlikely to exceed a peak of 9 Mbytes per second, and the very large buffer memory provided can hold over 80 full-length packets in a queue. Depending on the design of the carrier board, it may be advisable to use DMA transfers, particularly in special applications where high throughput is required, and when duplex operation is permitted.

3.7. Fast Ethernet™ Controller

The SMC 91C100 "Feast" is a controller for Fast Ethernet at 100 Mbits per second, supporting the IEEE 802.3u standard for 100BASE-T. Physical interface adaptors, external to the IP, for 100BASE-TX, 100BASE-T4 and 100BASE-FX can be driven. The interface to these is the media-independent interface (MII) defined in IEEE 802.3u-1995 (Supplement to the 802,3 documents) Clause 22.

So as to make the module more versatile, the controller also supports operation at 10 Mbps, to the 10BASE-T standard, again using an external physical-layer adaptor.

Full details of the operation of the 91C100 are given in the SMC data book, also available on the ACTIS reference CD ROM, and these must be consulted if a software driver is to be written.

The description given in this section does not go into complete detail, apart from those elements in the IP design which are not part of the 91C100 itself.

The 128 kbyte buffer memory is managed in a very efficient and flexible way. Normally, the controler allocates memory between transmission and reception automatically, but the user may request that an area of memory, such as 8k, 16k, or 32k bytes be reserved for transmission packet storage.

For each packet to be transmitted, the host software requests a buffer area - not needing to specify the size - and the 91C100 returns a packet number code. The user then sets a pointer and loads data, through the data registers and via FIFO buffers, into memory. The first word in the block is reserved for a status word which will be written after transmission, the second word is a byte count, and the following words constitute the data packet starting with the destination address. The source address is NOT supplied by the 91C100: it must be included in the packet written by the user. Normally, it will be copied from the address found in the IAR registers of the 91C100 after initialisation.

It is possible to set up several packets and initiate transmission by a single command, using a single interrupt when all have been sent. This may improve efficiency in some situations.

The process is similar for reception. Each received packet is given a serial number, and may be accessed through the data registers by setting up the pointer control word.

The first word in the memory buffer is a status word, including the 6-bit code from the CRC which governs the multi-cast feature. When the packet has been read, ir if it is to be discarded, a command must be ussied to remove it from the queue and this will present the next packet (if these is one) at the FIFO.

Each IEEE 802 controller board is issued with a unique 48-bit address set up by the manufacturer. In the LAN-100, this is stored in a small E^2PROM of 64 words x 16 bits, during production test. It is automatically loaded into the IAR registers of the 91C100. The user need never worry about access to the E^2PROM: if it is desired to load some data into the 61 spare locations then the procedure is described in the 91C100 data sheet.

Reception modes may be chosen from various options. The normal mode is to receive packets which have a destination address corresponding directly to that of the module. For multicast reception, an 8-byte table defines 64 control bits. The MSB 6 bits of the CRC code point to a bit, which if set enables the packet to be received. An option by which all packets of multicast type, i.e. with the first bit of the destination address set to 1, are received may be set. It is also possible to set a "promiscuous" mode in which all packets on the network are received: this is useful for monitor equipment, obtaining statistics on traffic, etc. and also for bridges and routers.

Full duplex operation may be enabled, and if this is not done the controller will not receive packets which it has itself transmitted. Full-duplex operation requires connection to hubs or other stations with appropriate capability.

Interrupts can be generated by 7 different events, with individual mask control, these are:

- allocation of memory for transmission
- transmission of one packet
- transmit FIFO empty (after sending a group of packets)
- reception of a packet
- early reception of a packet (when some part has been received, exceeding a programmable threshold)
- receive buffer overflow (lack of memory)
- the sum of a series of minor events.

3.7.1. Special Features.

The 8-bit interrupt vector register, at offset $21, may be read as well as written to. The interrupt line taken from the 91C100 is "INTR1" and must be enabled by writing $B2 to the CR (Bank 1 Offset 0). It is disabled on reset, and may be disabled dynamically by writing a code such as $B0. (It is also necessary to enable the individual types of interrupt as listed in the preceding section.) The IntReq0* line of the IP interface is driven.

The special register which enables no-wait-state operation in 8 MHz systems is described in Section 3.5 above.

DMA operation is provided, for one channel only using DMARQ0*. The DMA facilities of the 91C100 are not used, as they only function in 32-bit systems. Instead, a pseudo-DMA operation has been provided, by which DMA access is converted into access to the data register at offset $08. In order to use this, the DMA controller should be set up for external requests, with the byte count fixed by the host as there is no end-of-transfer signal generated by the IP. The register bank 2 of the 91C100 must be selected, and then a DMA request issued by writing $01 to offset $25. If a byte swap is desired, the DMA control register should be set to $05. At the end of the transfer the control register must be cleared to remove the outstanding request.

This process may not be necessary, if the host DMA controller is able to function without requests from the IP, by programming access to the register at offset $08 (or $18). In either case, it is important to maintain selection of register bank 2 during the transfer, perhaps by disabling interrupts. The IP is able to function at
12.8 MBytes per second as outlined in Section 3.5 above, in 32 MHz systems.

3.7.2. The Media Interfaces.

The primary interface to the physical layer, at 100 Mbits per second, is the standard MII interface, although implemented on a 50-pin connector as defined for IP module rather than the 40-pin connector.

This interface transmits data in both directions in 4-bit paths at 25 M symbols/second. It is media-independent, in that various types of transmission may be implemented.

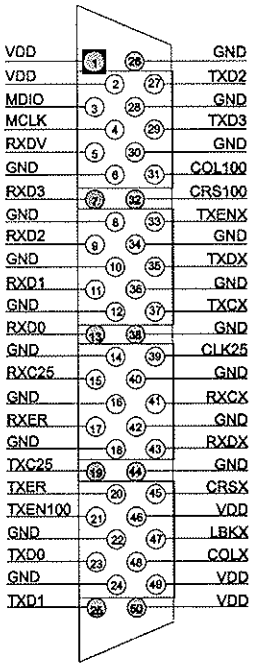
The primary method expected to be used is 100BASE-TX, which is a serial transmission at 100 MHz, but the interface is designed to handle a fibre-optic transceiver which is the same as that used in the F.D.D.I scheme. This transmits each 4-bit symbol as a 5-bit code, at 125 MHz. A further possibility is the 100BASE-T4 scheme, using 4-pair cables.

A 10 Mbps interface is also present on the 50-pin connector, and is intended for a combined 10/100 Mbps twisted-pair cable adaptor such as the LN100. Data is transmitted in serial NRZ form across this interface.

The MII includes a management interface for the external adaptors. This is a serial interface, using a software-generated clock and a bi-directional data line.

Data transfers can specify read or write to up to 32 external registers of 16 bits. (See appendix 1 for details of the registers in the LN-100 physical-layer adaptor, or IEEE Std. 802.3u-1995 for a general discussion.)

3.8. P2 Connection



The interface connection is not compatible with the I/O connection standard using a 50-pin connector to the IP specification. An adaptor module (LN-100) from ACTIS Computer is available for a easy connection to Category 5 twisted pair cables. A common RJ-45 connector is provided for both 10BASE-T and 100BASE-TX modes. The adaptor is made to mount on a 3U x 4TE front panel: 6U available to special request.

The interface cable should be as short as possible, preferably less than 300 mm (12").

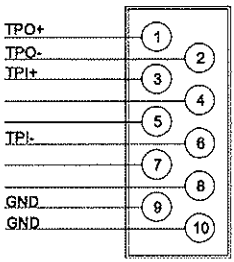
Signal codes ending in 'X' refer to the 10 Mbps option, while the others refer to the standard MII signal codes for the 100BASE-T adaptors.

Signal	I / O	Description
10 Mbps interface		
TXDX	O	transmit data
RXDX	I	receive data
TXCX	I	Transmit clock
RXCX	I	Receive clock
TXENX	O	Transmit enable
CRSX	I	Carrier sens
LBKX	O	Loopback
COLX	I	Collision

Signal	I / O	Description
100 Mbps interface (MII interface)		
TXD3-TXD0	O	Transmit clock
RXD3-RXD0	I	Receive clock
TXC25	I	Rransmit clock
RXC25	I	Receive clock
CLK25	O	25 MHz system clock
TXEN100	O	Transmit enable
TXER	O	Transmit error (typicaly VDD)
RXER	I	Receive error
MDIO	I/O	Management data I/O
MCLK	O	Management clock
RXDV	I	Receive data valid
COL100	I	Collision detect
CRS100	I	Carrier sense
General		
VDD	O	+5V @ 500 mA, fuse protected
GND	O	Ground

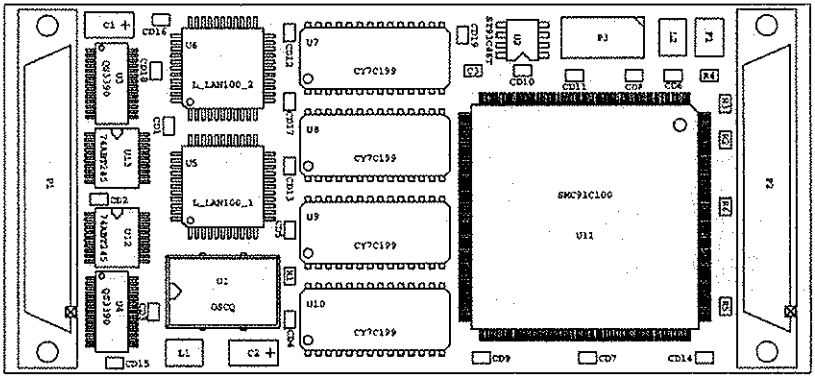
3.9. RJ-45 Connection

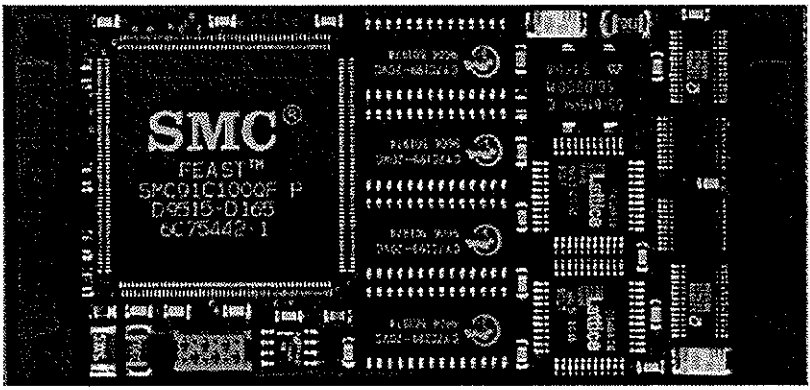
The following figure gives the RJ-45 pinout for both 10Base-T and 100Base-TX.



Signal	I / O	Description
TPO±	O	Twisted-Pair output
TPI±	I	Twisted-Pair input
GND	O	Ground

3.10.Component Location





4. APPENDIX
LN-100 Adaptor for PHY Interface.

4.1. Description.

This small module provides the transceivers for the twisted-pair interfaces, using a common RJ-45 connector.

It is based on the Micro-Linear ML6692 device, coupled with the ML2653 circuit for the 10BASE-T functions. Switching between 100 and 10 Mbps may be automatic, or software-selected.

The adaptor supports an automatic link protocol negotiation as defined in the IEEE 802.3u standard. The link test pulse scheme has been extended to signal capabilities between entities at either end of the cable, for 10 and 100 Mbps functions.

Four LED indicators are provided, for:

- 100BASE-TX enabled
- Collision
- 10BASE-T enabled
- 10BASE-T tx/Rx activity

It is connected to the LAN-100 IP module using a 50-pin connection which includes the IEEE 802.3u-1995 standard media-independent interface (MII) for the 100BASE-TX functions, with extra signals for 10BASE-T operation.

4.2. Management Functions.

4.2.1. Overview:

There are 5 registers provided:

Address	Register description
0	Control register
1	Status register
4	Advertisement register
5	Link partner register
6	Expansion register.

4.2.2. Formats:

Commands must use a serial format commencing with a series of at least 32 "1"'s of data, with clock pulses having at least 400ns period. The frame then starts with 0101 for a Write, or 0110 for Read, followed by 10 address bits PHYAD (5 bits all at 0 in this case), and REGAD (A4 to A0) for the register selection.

The first part of the frame is followed by a 2-bit "turn-round" gap, where for a read command the master tri-states its output, and the slave sends a "0" in the second of these bits. For writing the master sends 1, then 0.

Sixteen bits of register data are then sent, m.s. bit first.

Data is TTL positive logic, and is set by the master near to the negative transition of the clock and sampled on the positive clock edge. Data returned from the slave is set up to 300ns after the positive edge of the clock, and can be sampled by the master just before it sets the clock high for the subsequent pulse.

4.3. ML6692 REGISTERS

4.3.1. CONTROL REGISTER

BIT(s)	NAME	DESCRIPTION	R/W	DEFAULT
0.15	Reset	1 = reset all register bits to defaults 0 = normal operation	R/W, SC	0
0.14	Loopback	1 = PMD loopback mode 0 = normal operation	R/W	0
0.13	Manual speed select (Active when 0.12 = 0)	1 = 100Mb/s 0 = 10Mb/s	R/W	1
0.12	Auto negotiation enable	1 = enable auto negotiation 0 = disable auto negotiation	R/W	1
0.11	Power down	1 = power down 0 = normal operation	R/W	0
0.10	Isolate	1 = electrically isolate the ML6692 from MII 0 = normal operation	R/W	1
0.9	Restart auto negotiation	1 = restart auto negotiation 0 = normal operation	R/W, SC	0
0.8	Duplex mode	1 = Full duplex select, auto negotiation disabled 0 = Half duplex select, auto negotiation disabled	R/W	0
0.7	Collision Test	1 = enable COL signal test 0 = normal operation	R/W	0

4.3.2. STATUS REGISTER

BIT(s)	NAME	DESCRIPTION	R/W	DEPENDS ON DEFAULT PROGRAMMING
1.15	100BASE-T4	1 = 100BASE-T4 capability 0 = no 100BASE-T4 capability	RO	SEL100T4
1.14	100BASE-TX full duplex	1 = full duplex 100BASE-TX capability 0 = No full duplex 100BASE-TX capability	RO	1
1.13	100BASE-TX half duplex	1 = half duplex 100BASE-TX capability 0 = no half duplex 100BASE-TX capability	RO	1
1.12	10Mb/s full duplex	1 = full duplex 10Mb/s capability 0 = No full duplex 10Mb/s capability	RO	SEL10FDUP
1.11	10BASE-T (half duplex)	1 = 10BASE-T (half duplex) capability 0 = No 10BASE-T (half duplex) capability	RO	SEL10HDUP
1.5	Auto negotiation compl.	1 = auto negotiation process complete 0 = auto negotiation not complete	RO	0
1.3	Auto negotiation ability	1 = auto negotiation capability available 0 = auto negotiation capability not available	RO	1
1.2	Link status	1 = one and only one PHY-specific link is up 0 = link is down link fail until read	RO/L L	latch low after
1.0	Extended capability	1 = extended register capabilities 0 = basic register set only registers)	RO	1 (auto neg.

4.3.3. ADVERTISEMENT REGISTER

BIT(s)	NAME	DESCRIPTION	R/W	DEPENDS ON DEFAULT PROGRAMMING
4.15	Next Page	1 = additional link code word pages 0 = no additional pages	RO	0
4.14	Reserved	Write as zero, ignore on read	RO	
4.13	Remote fault	1 = remote wire fault detected 0 = no remote wire fault detected	R/W	0
4.12-4.10	Reserved	(Not used at present)		
4.9	100BASE-T4 capability	1 = 100BASE-T4 capability 0 = no 100BASE-T4 capability	R/W	SEL100T4
4.8	100BASE-TX full duplex	1 = 100BASE-TX full duplex capability 0 = no 100BASE-TX full duplex	R/W	1
4.7	100BASE-TX	1 = 100BASE-TX capability 0 = no 100BASE-TX capability	R/W	1
4.6	10BASE-T full duplex	1 = 10BASE-T full duplex capability 0 = no 10BASE-T full duplex capability	R/W	SEL10FDUP
4.5	10BASE-T	1 = 10BASE-T capability 0 = no 10BASE-T capability	R/W	SEL10HDUP
4.4-4.1	Selector field	All these bits are 0 for 802.3 LANs	RO	0
4.0	Selector field	This bit is a 1 for 802.3 LANs	RO	1

4.3.4. LINK PARTNER REGISTER

BIT(s)	NAME	DESCRIPTION	R/W	DEFAULT
5.15	Next Page	1 = additional link code word pages 0 = no additional pages	RO	X
5.14	Acknowledge	1 = link partner's successful receipt of local station code 0 = no link partner reception of local station code	RO	X
5.13	Remote fault	1 = remote wire fault detected 0 = no remote wire fault detected	R/W	X
5.12-5.10	Reserved	(Not used at present)	X	
5.9	100BASE-T4 capability	1 = 100BASE-T4 capability 0 = no 100BASE-T4 capability	R/W	X
5.8	100BASE-TX full duplex	1 = 100BASE-TX full duplex capability 0 = no 100BASE-TX full duplex	R/W	X
5.7	100BASE-TX	1 = 100BASE-TX capability 0 = no 100BASE-TX capability	R/W	X
5.6	10BASE-T full duplex	1 = 10BASE-T full duplex capability 0 = no 10BASE-T full duplex capability	R/W	X
5.5	10BASE-T	1 = 10BASE-T capability 0 = no 10BASE-T capability	R/W	X
5.4-5.1	Selector field	All these bits are 0 for 802.3 LANs	RO	X
5.0	Selector field	This bit is a 1 for 802.3 LANs	RO	X

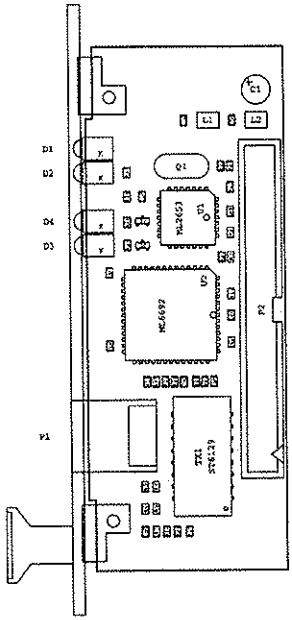
4.3.5. EXPANSION REGISTER

BIT(s)	NAME	DESCRIPTION	R/W	DEFAULT
6.15-6.5	Reserved; not used			0
6.4	Multiple link fault	1 = more than one receiving protocol indicates link OK on read 0 = no multiple link faults	RO; reset	0
6.3	Link partner next page able	1 = link partner supports next page 0 = link partner has no next page	RO	0
6.2	Next page able	1 = local port supports next page 0 = local port has no next page	RO	0
6.1	Page received	1 = 3 identical, consecutive link code words received on read 0 = 3 identical, consecutive link code words NOT received	RO; reset	0
6.0	Link partner auto neg. Capable	1 = link partner has auto negotiation capability 0 = link partner has NO auto negotiation capability	RO	0

NOTE: All unnamed or unused register locations will return 0 values when accessed.

KEY: LL = latch low until read, R/W = read/write, RO = read only, SC = self-clearing.

4.4. Component Location



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