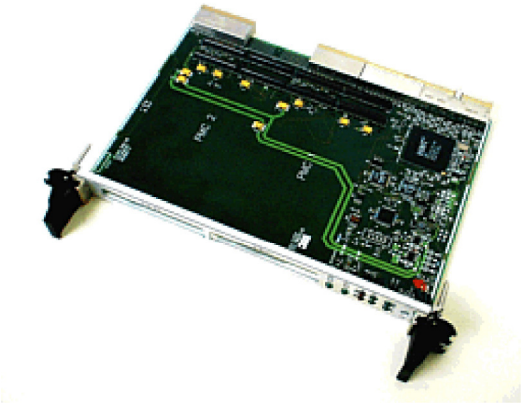
Dual PCI Mezzanine Card (PMC) Carrier for CompactPCI with full Hotswap capabilities



The cPC2PMC64 is a hot swap 66MHz 64-bit CompactPCI® dual PCI Mezzanine Card (PMC) carrier. It is possible to remove the cPC2PMC64 and associated PMC modules from a live powered CompactPCI® system without having to power down the system first. The on-board PCI bridge fully supports the latest PICMG programming specifications and its device hiding capabilites ensure trouble free operation under hotswap conditions.

Two versions are available with rear I/O routed to either J3 and J4 or to J3 and J5 for use in systems with the H110 bus present on the backplane.

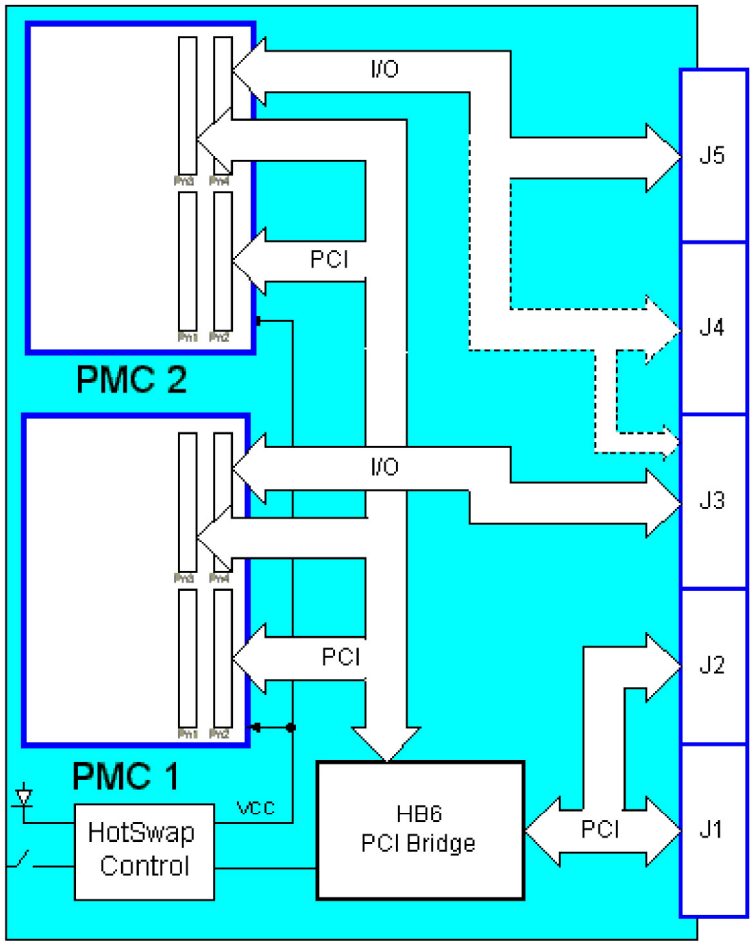
Features

- HiNT HB6 66MHz 64-bit PCI bridge conforming to PCI local bus specification 2.2.
- Compatible with CompactPCI® Specification 2.0 R3.0.
- Compatible with CompactPCI® Hot Swap Specification 2.1 R2.0.
- Compatible with PMC on CompactPCI® Specification PICMG 2.3 R1.0 (cPC2PMC64).
- Compatible with CompactPCI® Computer Telephony Specification 2.5 R1.0 (cPC2PMC64-T).
- Supports CompactPCI® Hot Swap "High Availability Programmers Interface Level 1.
- Supports CompactPCI® Hot Swap "Device Hiding" to eliminate mid-transaction extractions.
- Two PMC sites conforming to PMC standard IEEE 1386.1.
- Power to both PMC sites controlled by single chip Hot Swap controller (LTC1643).
- PMC rear I/O via J3 & J4 (cPC2PMC64) or J3 & J5 (cPC2PMC64-T).

Applications

- General purpose 66MHz 64-bit carrier for PMC modules.
    - Supports a wide range of industrial I/O PMC modules.
    - High performance PMC I/O (serial, SCSI, Ethernet etc.).
- Hot-swappable carrier for PMC modules.
    - Extraction & insertion in live systems.
- Telephony systems compatible PMC carrier (cPC2PMC64-T).

    - J4 available for H110 CT bus.



Block Diagram

CompactPCI® Interface

The CompactPCI® interface on the cPC2PMC64 is implemented using a HiNT HB6 PCI-to-PCI Bridge. This provides a high performance connection path between the CompactPCI® bus and the on-board PCI bus. The HB6 also supports high availability applications, frequency conversions, high availability hot swap enabling and universal system-to-system bridging. The HB6 has sophisticated buffer management and buffer configuration options designed to provide customisable performance optimisation

The HB6 bridge is compliant with the PCI Local Bus Specification, overcoming the electrical loading limits on the PCI bus by creating hierarchical buses. It also provides internal arbitration for the secondary bus masters.

The HB6 provides CompactPCI® (CPCI) hot-swap extended capability allowing live insertion and extraction of the cPC2PMC64 CompactPCI® Hot Swap Dual PMC Carrier. It is compliant with the PCI-to-PCI Bridge Specification Revision 1.1 and PCI Power Management Interface Specification Revision 1.0.

PCI-to-PCI Bridge Features

- PCI Local Bus Specification 2.2 support.
- High speed PCI buffer supports 3.3V signalling with 5V input signal tolerance.
- CPCI Hot Swap Specification PICMG 2.1 R2.0 with PI = 1 support.
- Device Hiding support eliminates mid-transaction extraction problems.
- Programmable 32-bit to 64-bit access conversion.
- Flow-Through 0 wait state burst up to 4K bytes for optimal large volume data transfer.
- Supports up to 4 simultaneous posted write transactions in each direction.
- Supports up to 4 simultaneous delayed transactions in each direction.
- Provides 1K bytes of buffering:
    - 256 byte upstream posted write buffer
    - 256 byte downstream posted write buffer
    - 256 byte upstream read data buffer
    - 256 byte downstream read data buffer
- Programmable prefetch amount of up to 256 bytes for maximum read performance optimisation.
- Supports out of order delayed transactions.

- Supports upstream and downstream lock.
- Serial EEPROM loadable and programmable PCI READ ONLY register configurations.
- External arbiter or programmable arbitration for 9 bus masters on secondary interface support.
- PCI Mobile Design Guide and Power Management D3 Cold Wakeup capable with PME# support.
- Enhanced address decoding:
    - Support 32-bit I/O address range.
    - 32-bit memory-mapped I/O address range.
    - ISA aware mode for legacy support in the first 64K bytes of I/O address range.
    - VGA addressing and palette snooping support.
- Asynchronous design supports standard 66MHz to 33MHz and faster secondary port speed such as 33MHz to 66MHz conversion.

CompactPCI® Bus Connection

The cPC2PMC64 is a 66MHz 64-bit compatible CompactPCI® module that will also operate in 33MHz and 32-bit applications. The CompactPCI® enclosure can be standard, Hot Swap or High Availability. The cPC2PMC64 can be used in a CompactPCI® enclosure with up to 8 slots @ 33MHz (3.3V or 5V VI/O) or 5 slots @ 66MHz (3.3V VI/O) without any setting changes. The CompactPCI® VI/O setting has no effect on the PMC sites.

PMC Sites

Two 66MHz 64-bit PMC sites are provided which are also fully compatible with 33MHz 32-bit PMC modules. These sites conform to "Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC, IEEE1386.1" and "Standard for a Common Mezzanine Card Family: CMC IEEE1386".

I/O Voltage

The VI/O voltage to the PMC sites is link selectable to +3.3V or +5V VI/O. This VI/O is independent of the CompactPCI® backplane VI/O. The +5V PCI VI/O to the PMC site is only be required for older +5V only PMC modules. The cPC2PMC64 PMC sites can be keyed for +3.3V or +5V operation, depending on the PCI VI/O setting. This only affects the levels of the signals on the PCI bus, the cPC2PMC64 always provides -12V, +12V, +5V and +3.3V supplies to the PMC sites.

PMC Bus Connection

The cPC2PMC64 supports 33MHz or 66MHz, 32-bit or 64-bit PMC modules, but note that the on-board PCI bus will operate to the least performance PMC module for both PMC modules.

Hot Swap Controller

The cPC2PMC64 uses a Linear Technology LTC® Hot Swap™ controller that allows the cPC2PMC64 to be safely inserted and removed from a live CompactPCI® slot. Four external transistors control the 3.3V, 5V, 12V and -12V supplies. All supply voltages are ramped up at a controlled rate to prevent any current glitches.

An electronic circuit breaker protects all four supplies against overcurrent faults. The foldback current limit feature limits current spikes and power dissipation when shorts occur and the cPC2PMC64 to be powered up without tripping the circuit breaker.

The PWRGD output indicates when all of the supply voltages are within tolerance and drives the CompactPCI® HEALTHY# signal. The ON pin is driven from the CompactPCI® BD_SEL# signal and is used to cycle the board power or reset the circuit breaker.

Hot Swap Controller Features

- Allows safe board insertion and removal from a live CompactPCI® slot.
- Controls 3.3V, 5V, 12V, -12V supplies.
- Foldback current limit with circuit breaker.
- Ramped supply voltage power-up.
- High-side drive for external N-channels.
- Fault and power-good outputs.

Ejector Handle Switch Operation

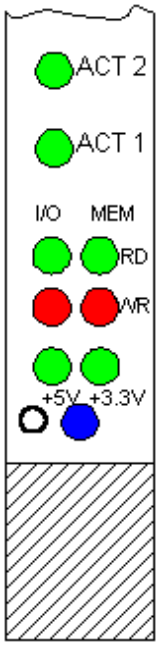
The cPC2PMC64 uses a microswitch built in to the lower front-panel ejector/injector handle. A change of state in the microswitch will occur during an insertion and extraction from a CompactPCI® backplane. This will cause the ENUM# signal to be asserted on the CompactPCI® backplane.

LED Indicators

Nine LED indicators are fitted through the front panel, which can be viewed through the front panel of the cPC2PMC64. The functions are shown below.

Name	Colour	Function
ACT 2	GREEN	PMC site 2 is bus master
ACT 1	GREEN	PMC site 1 is bus master
I/O RD	GREEN	I/O or configuration read cycle
MEM RD	GREEN	Memory read cycle
I/O WR	RED	I/O or configuration write cycle
MEM WR	RED	Memory write cycle
+5V	GREEN	+5V present on PMC sites
+3.3V	GREEN	+3.3V present on PMC sites
O	BLUE	Lit when board may be removed

Front Panel Location



PCI LEDS

There are also four LED indicators fitted on the PCB showing the operational parameters of the primary PCI bus (CompactPCI®) and secondary PCI bus (PMC). Indicators show 66MHz if on (33MHz if off) and 64-bit if on (32-bit if off). These LEDS are intended to check the initial set-up for the board during installation.

Rear I/O Connectors J3, J4 and J5

cPC2PMC64

The two PMC sites (1 & 2) are connected to Pn4, and the CompactPCI® connectors J3 & J4. This is compatible with the PMC on CompactPCI® Specification PICMG 2.3 R1.0 and applies to the cPC2PMC64 (non-telephony version) *where connector J5 is not fitted*.

cPC2PMC64-T

The two PMC sites (1 & 2) are connected to Pn4, and the CompactPCI® connectors J3 & J5. This applies to the cPC2PMC64-T (telephony version) *where connector J4 is not fitted*. It is **NOT** compatible with the PMC on CompactPCI® Specification PICMG 2.3 R1.0 but is widely used in telephony applications to leave J4 free for the H110 telephony bus.

Programming

HB6 PCI-to-PCI Bridge

Support for the HB6 PCI-to-PCI Bridge is built into standard operating systems such as Windows and Linux.

PCI Subsystem Registers

The HB6 PCI-to-PCI Bridge supports both a Subsystem Vendor ID and Subsystem ID, which are loaded from EEPROM on reset and/or power-up. The EEPROM is supplied pre-programmed by BVM, and contains the BVM PCI Subsystem Vendor ID.

Specification

On-Board Functions

HB6 PCI-to-PCI Bridge

HiNT HB6 PCI-to-PCI Bridge.
PICMG 2.0 R3.0 CompactPCI® Compliant.
PICMG 2.1 R2.0 CompactPCI® Hot Swap Compliant.
PCI Local Bus Revision 2.2 Compliant.
PCI Bus Power Management Interface Revision 1.0.
Two 64-bit 66MHz PCI buses.

LTC®1643L Hot Swap Controller

Linear Technology LTC®1643L Hot Swap™ Controller.
PICMG 2.0 R3.0 CompactPCI® Compliant.
PICMG 2.1 R2.0 CompactPCI® Hot Swap Compliant.
± 12V, 3.3V & 5V switching with ramped power-up.

Board Configuration

Links:	PME# select; PMC VI/O select.
LED Indicators:	PMC activity; I/O read/write; memory read/write; +5V; 3.3V; hot swap ready; 64-bit primary PCI; 66MHz primary PCI; 64-bit secondary PCI; 66MHz secondary PCI.

CompactPCI® Interface

Bus Interface:	PCI Local Bus Revision 2.2 Compliant; PICMG 2.0 R3.0 CompactPCI® Compliant PICMG 2.1 R2.0 CompactPCI® Full Hot Swap Compliant
Bus Width:	64 & 32-bit.
Bus Speed:	66 & 33MHz.
Data Transfer:	PCI 2.2 Bus Mastering.
Interrupts:	PCI INT #A,#B,#C,#D.

PMC Interface

Bus Interface:	PCI 2.2 Compliant.
Bus Width:	64 & 32-bit.
Bus Speed:	66 & 33MHz.
Data Transfer:	PCI 2.2 Bus Mastering.
Interrupts:	PCI INT #A,#B,#C,#D.
I/O connection:	PICMG 2.3 R1.0 PMC on CompactPCI® Compliant (cPC2PMC64); PICMG 2.5 R1.0 CompactPCI® CT Compliant (cPC2PMC64-T).

Operating Environment

Dimensions:	160mm x 233.35mm (6U) single slot.
Power:	+3.3V TBDmA, +5V TBDmA typical (excluding PMC requirements).
Environmental:	0 to 70 ° C, 95% humidity non-condensing (extended range to order)

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