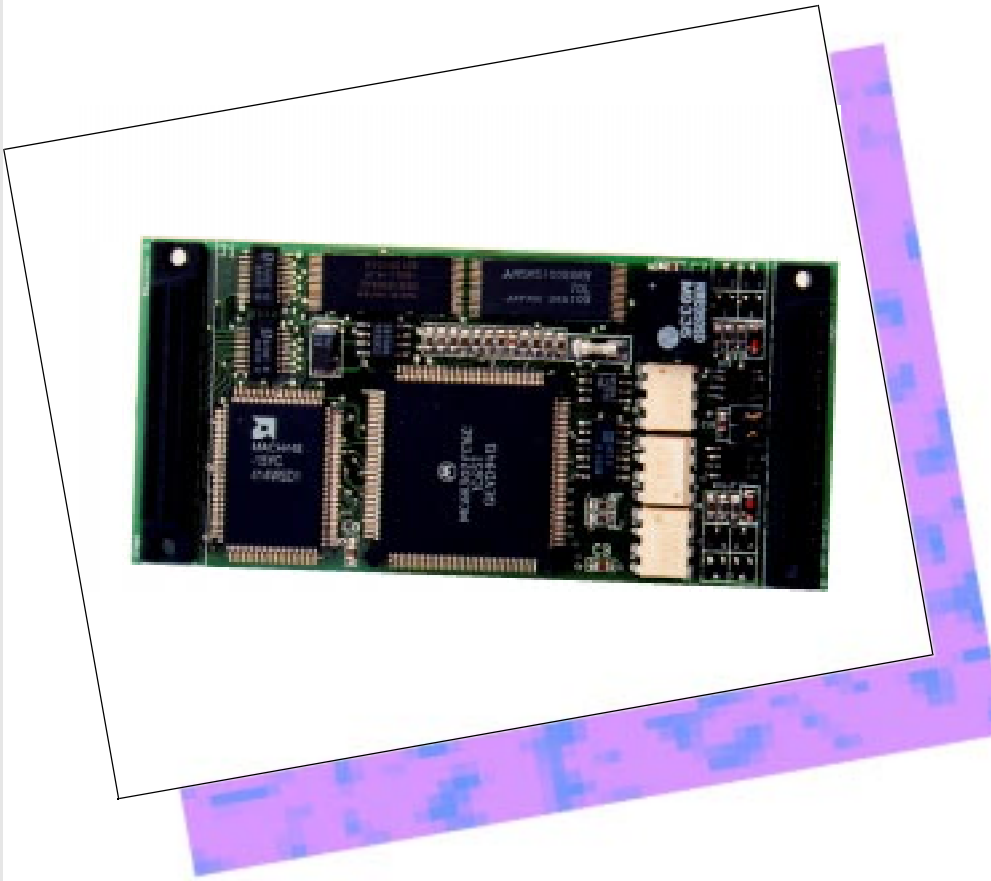
IP302

Intelligent I/O IndustryPack™

- 68302 Integrated Multi-protocol Processor (IMP)
- 16MHz Processor Clock
- One Opto-Isolated RS485 Serial Port with Synchronous and Asynchronous operation to 2Mbits/second transfer rates
- Additional general purpose unbuffered I/O pin's which can be configured as:-
  - 2 Serial ports
  - 2 Counter/Timers (cascadeable)
  - 1 Watchdog Timer
  - Up to 28 Digital I/O lines
- 256Kbyte 16 bit wide Dual Port Ram
- IP I/O used to control the 68302 Sleep State
- 68302 Interrupt generation to the IP Interface
- Programmable Interrupt Vector
- IP Interrupt generation to the 68302 (Autovectored level 1)
- Programmable non-volatile Station ID
- Supports Read-Modify-Write Cycles to the Dual-Port RAM from the Carrier Board
- 8MHz Single IP conforming to the IndustryPack™ Logic Interface Specification
- OS-9 Operating System and FieldLink networking software
- Comprehensive carrier hosted debug/monitor

The IP302 is a general purpose IndustryPack™ built around an 68302 Integrated Multi-protocol Processor. It features an on-board RS485 port, fully opto-isolated with transient suppression, operating over two/four wire asynchronously/synchronously. Speeds of up to 2 Mbits/second are achievable.



The IP302 is optimised for use as a gateway into BVM's FieldLink distributed fieldbus network but it finds many applications in other communication areas where the microcode of the 68302 offers many advantages.

In addition two further serial ports, two counter timers, a watchdog timer and 28 digital I/O lines are available as unbuffered TTL levels allowing the user to implement signal conditioning on an external transition module as required. Communication with the host IndustryPack™ carrier is via the Dual Ported SRAM which also holds the code for its firmware. The code for the firmware is downloaded following system boot up.

IP302

Processor

The IP302 is controlled by a 16MHz 68302 Integrated Multi-protocol Processor (IMP), which has a HCMOS 68000 core and a flexible communication architecture. All general purpose I/O lines are made available to the outside world, giving 3 serial ports, two counter/timers and a watchdog timer. All are available to the user.

Memory

The IP302 has 256Kbytes of 16-bit wide Dual Ported SRAM. The RAM is used to store the operation code for the 68302 and to pass data to and from the IMP's peripherals. It is zero wait stated on the CPU side, which arbitrates for the Bus with the IP carrier for control of the SRAM.

Serial Interface

One of the three available serial ports is used as the FieldlLink Gateway Port. SCC1 is configured to give an Opto-Isolated RS485 serial port accessed via the IP I/O connector. The port can transmit and receive both data and the clock to give synchronous and asynchronous operation at up to 2Mbits/second transfer rates. Two general purpose I/O lines are used to control the direction of the serial buffers. All the lines are also fed separately to the IP I/O connector and are available if this feature is not used.

IndustryPack™ Interface

The IP interface conforms to the IndustryPack™ Logic Interface Specification. The ID Prom is built into the Control Logic PLD and holds the IP ID Data. The PROM does not have any IP specific space or user space. The IP I/O space is used to control the 68302's sleep state. After an IP RESET the 68302 is held in sleep state (CPURESET asserted) so its firmware can be loaded into the Dual Ported RAM from the carrier board. When the loading is complete, the carrier sets a bit in the IP I/O space CPURUN register, which releases the 68302 from its sleep state (CPURESET negated) and allows it to run the code. If the 68302 firmware needs changing, the CPURUN register bit in the IP I/O space is cleared, returning the 68302 to sleep, and allowing the new code to be loaded into the Dual Port RAM.

The Dual Ported RAM is accessible as a 256Kbyte block in the IP Memory area, and is linearly accessed as 16-bit wide from both the 68302 and the IP interface. Read Modify Writes to the Dual Ported RAM from the IP Carrier are supported. If a register in the IP I/O space is set by the user to indicate a RMW cycle, the control logic will keep the bus to the RAM for two IP Memory accesses, once the processor has granted it. RMW cycles from the 68302 to the Dual Ported RAM are handled automatically.

The IP302 has an onboard EEPROM which stores the station ID. The EEPROM can be accessed by the 68302 via its IP Control Register space. Two registers are used to access the device, a CONTROL and DATA IN register to write to the device, and a DATA OUT register to read data.

Interrupts

The 68302 can be programmed to cause an IP interrupt on the INTREQ0 line. The 68302 writes the Vector number into the vector Register causing a bit to be set in an IP Interrupt register in the IP I/O space and an interrupt occurs. The Interrupt is cleared by writing to the IP Interrupt register in the IP I/O space, if an IP RESET occurs or if the 68302 is put back to sleep. The IP interrupt status can be checked by reading the IP Interrupt I/O register

A local 68302 autovectored level 1 interrupt can be generated by accessing the IP I/O space. The IP carrier writes a bit to the CPU Interrupt Register in its IP I/O space causing a CPU interrupt to be generated. The Interrupt is cleared by 68302, writing to the CPU Interrupt register in the IP Control Register space or if the 68302 is put back to sleep. The 68302 interrupt status can be checked by reading CPU Interrupt I/O register.

Firmware

All firmware for the IP302 is downloaded from the host carrier. A complete port of FieldLink is available which provides the interconnectivity of the host OS-9 system to the FieldLink fieldbus network.

For users wishing to produce their own firmware a two part debugger is available. This debugger is optimised to use minimum space on the IP302, whilst providing a comprehensive command set, by running most of its code on the host systems CPU.

Specification

Logic Interface
IndustryPack™ Logic Interface

Interrupt
INTREQ0 CPU Source, RORA

Registers
CPURUN
IP Interrupt Status
CPU Interrupt Enable
CPU Interrupt
Dual Port RAM Read Modify Write Enable

Controller
MC68302 Integrated MultiProtocol Processor with 16Mhz clock

Serial Port
1 x Opto-Isolated RS485 Port with Multi-drop Clock Signals

Additional I/O Options
2 Serial ports. (TTL)
2 Counter Timers (cascadeable)
1 Watchdog Timer
Or
Up to 28 Digital I/O lines depending on the Peripherals used
All I/O available through IP I/O connector

Bus Timeout
Programmable 8µS to 1mS

Watchdog
Programmable 0.5ms to 16.67S

Reset
Controlled by IP I/O Register CPURUN

Interrupt
IRQ1 Source (Autovectored) RORA

Registers
IP Interrupt Vector
EEPROM Data In/Control
EEPROM Data Out
CPU Interrupt Status

Dual Ported RAM
256Kbytes of CMOS SRAM 16-bit wide

Links
RS485 Data Termination Select
RS485 Clock Termination Select

Dimensions
45.72mm x 99.06mm Single IndustryPack Size

Power
+5V 500mA typical
±12V 0mA

Environmental
0 to 70° C
5-95% humidity non-condensing
(other ranges to order)

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