

HIGHLIGHTS

ARCHITECTURE LEADERSHIP

■ BASED ON AMD INFINITY ARCHITECTURE, new 2nd Gen AMD EPYC™ Processors are the first server processors featuring 7nm hybrid multi-die design and PCle® Gen4. The AMD EPYC Family continues to offer the most I/O and memory bandwidth¹ in its class.

PERFORMANCE LEADERSHIP

WITH UP TO 64 HIGH PERFORMANCE CORES PER SOC, 2nd Gen AMD EPYC Processors deliver world-record², best-inclass performance up to a 2x³ generational performance increase that outpaces Intel Xeon Platinum by up to 102%⁴.

SECURITY LEADERSHIP

ADVANCED SECURITY FEATURES
AND A SILICON-EMBEDDED
SECURITY SUBSYSTEM, 2nd Gen
AMD EPYC Processors are 'hardened
at the core,' helping customers
guard their most important assets—
their data. New 2nd Gen AMD EPYC
processors, cryptographically isolate
and secure more than 500 virtual
machines per server using AMD
Secure Encrypted Virtualization
with no application changes
required.

AMD EPYC™ 7002 Series Processors: A New Standard for the Modern Datacenter

Architecture. Performance. Security. AMD EPYC 7002 Series Processors set a new standard for the modern datacenter. They help turbocharge your application performance, transform datacenter operations, and help secure mission-critical data.

AMD EPYC 7002 Series Processors set a new standard for the modern datacenter. Driven by the AMD Infinity Architecture, the AMD EPYC 7002 Family is the first x86-architecture server processor based on 7nm process technology, a hybrid, multi-die architecture, PCIe® Gen4 I/O, and an embedded security architecture. Together, these innovative capabilities deliver what you need. Performance leadership for your workloads. Security features at every layer to help protect your CPU, applications, and data—whether in your enterprise datacenter or the public cloud. And with the range of features you need to power your datacenter, you can adapt your IT infrastructure to match workload challenges you face today and into the future.

AMD EPYC INFINITY ARCHITECTURE

AMD Infinity Architecture embodies AMD's leadership philosophy in its EPYC processor designs. It is the reason that AMD EPYC processors have leaped ahead of the market again and it is the reason to expect AMD processors to stay ahead in the future.

A BETTER DESIGN WITH INDEPENDENT PATHS FOR INNOVATION

AMD EPYC 7002 Series Processors leapfrog the industry by using a 7nm process for the CPU cores and a 14nm process for I/O, memory access, and security functions. A system-on-chip (SoC) design eliminates the need for many external support chips, helping reduce capital and server design costs. An "all-in" feature set delivers a uniform set of features regardless of the number of processor cores.

PERFORMANCE LEADERSHIP

Accelerated performance comes from a commitment to greater parallelism. With up to 64 cores per SOC and "Zen 2" features, the AMD EPYC 7002 Series surpasses 1st Gen AMD EPYC Processor with improved execution pipelines, higher clock rates, and up to 4x the shared Level 3 cache. The result is more than twice the performance³ and up to 4x the theoretical peak floating point operations per second⁵ (FLOPS) when compared to 1st Gen AMD EPYC Processors. The processors claim world-record performance² across major industry benchmarks including SPEC CPU® 2017, TPC®, and VMware® VMmark® 3.1.

AMD EPYC 7002 Series Processors



BETTER TOGETHER

Pairing these innovative processors with the world's first 7nm process GPU accelerator, the AMD Radeon Instinct™ MI50 and MI60, you can accelerate HPC, data analytics, artificial intelligence, and machine learning workloads. Because our 7nm technology reduces the size of each CPU core, you can enjoy

the same level of performance with roughly half the energy consumption⁶. The combination of DDR4-3200 DIMMs and more memory bandwidth increases the flow of data between memory and the processor so that your applications can access information faster and shorten time to results.

| Model | Cores | Threads | Base Freq. (GHz) | Max. Boost Freq.(GHz) ^a (Up to) | TDP (W) | L3 Cache (MB) | DDR Channels | Max DDR Freq. (1DPC) | Per-Socket Theoretical Memory Bandwidth (GB/s) | PCIe® Gen 4 Lanes | 2P/1P |
|-------|-------|---------|---------------------|--|--------------------|------------------|-----------------|-------------------------|--|-------------------------|---------|
| 7H12 | 64 | 128 | 2.6 | 3.3 | 280 ^{c,d} | 256 | 8 | 3200 | 204.8 | 128 | 2P/1P |
| 7742 | 64 | 128 | 2.25 | 3.40 | 225° | 256 | 8 | 3200 | 204.8 | 128 | 2P/1P |
| 7702 | 64 | 128 | 2.00 | 3.35 | 200 | 256 | 8 | 3200 | 204.8 | 128 | 2P/1P |
| 7702P | | | | | | | | | | | 1P only |
| 7662 | 64 | 128 | 2.00 | 3.30 | 225c | 256 | 8 | 3200 | 204.8 | 128 | 2P/1P |
| 7642 | 48 | 96 | 2.30 | 3.30 | 225° | 256 | 8 | 3200 | 204.8 | 128 | 2P/1P |
| 7552 | 48 | 96 | 2.20 | 3.30 | 200 | 192 | 8 | 3200 | 204.8 | 128 | 2P/1P |
| 7542 | 32 | 64 | 2.90 | 3.40 | 225° | 128 | 8 | 3200 | 204.8 | 128 | 2P/1P |
| 7532 | 32 | 64 | 2.40 | 3.30 | 200 | 256 | 8 | 3200 | 204.8 | 128 | 1P/1P |
| 7502 | 32 | 64 | 2.50 | 3.35 | 180 | 128 | 8 | 3200 | 204.8 | 128 | 2P/1P |
| 7502P | | | | | | | | | | | 1P only |
| 7452 | 32 | 64 | 2.35 | 3.35 | 155 | 128 | 8 | 3200 | 204.8 | 128 | 2P/1P |
| 7402 | 24 | 48 | 2.80 | 3.35 | 180 | 128 | 8 | 3200 | 204.8 | 128 | 2P/1P |
| 7402P | | | | | | | | | | | 1P only |
| 7352 | 24 | 48 | 2.30 | 3.20 | 155 | 128 | 8 | 3200 | 204.8 | 128 | 2P/1P |
| 7302 | 16 | 32 | 3.00 | 3.30 | 155 | 128 | 8 | 3200 | 204.8 | 128 | 2P/1P |
| 7302P | | | | | | | | | | | 1P only |
| 7282 | 16 | 32 | 2.80 | 3.20 | 120 | 64 | 8 | 3200 | 85.3⁵ | 128 | 2P/1P |
| 7272 | 12 | 24 | 2.90 | 3.20 | 120 | 64 | 8 | 3200 | 85.3⁵ | 128 | 2P/1P |
| 7262 | 8 | 16 | 3.20 | 3.40 | 155 | 128 | 8 | 3200 | 204.8 | 128 | 2P/1P |
| 7252 | 8 | 16 | 3.10 | 3.20 | 120 | 64 | 8 | 3200 | 85.3⁵ | 128 | 2P/1P |
| 7232P | 8 | 16 | 3.10 | 3.20 | 120 | 32 | 8 | 3200 | 85.3⁵ | 128 | 1P only |

- a. Max boost for AMD EPYC processors is the maximum frequency achievable by any single core on the processor under normal operating conditions for server systems. EPYC-18
- b. Performance optimized for 4 channels with DDR4-2667 DIMMS. Additional memory channels will not increase overall memory bandwidth.
- c. Some supported features and functionality of 2nd Gen AMD EPYC processors require a BIOS update from your server manufacturer when used with a motherboard designed for 1st Gen AMD EPYC Processors. A motherboard designed for 2nd Gen AMD EPYC Processors is required to enable all available functionality. ROM-06
- d. AMD EPYC 7H12 processor boost frequencies may be achieved only with a cooling solution that meets group 'Z' requirements. Achievable boost frequencies may vary depending on the effectiveness of the actual cooling solution. ROM-282

FOOTNOTES

- 1. EPYC 7002 series has 8 memory channels, supporting 3200 MHz DIMMs yielding 204.8 GB/s of bandwidth vs. the same class of Intel Scalable Gen 2 processors with only 6 memory channels and supporting 2933 MHz DIMMs yielding 140.8 GB/s of bandwidth. 204.8 / 140.8 = 1.454545 1.0 = .45 or 45% more. AMD EPYC has 45% more bandwidth. Class based on industry-standard pin-based (LGA) X86 processors. ROM-11
- 2. For a complete list of world records see http://amd.com/worldrecords. ROM-169
- 3. 1-n, 2-socket 2nd Gen EPYC 7H12 powered server (http://spec.org/cpu2017/results/res2019q4/cpu2017-20190918-18501.html) scoring 695 SPECrate 2017_int_base has up to 2.29X the SPECrate 2017 Integer (Base) performance of the highest previous generation score of 304 SPECrate 2017_int_base by a 1-n, 2-socket 1st Gen EPYC 7601 powered server result (http://www.spec.org/cpu2017/results/res2019q2/cpu2017-20190411-11817.html as of 11/13/19. ROM-342
- 4. 2P 2nd Gen EPYC™ 7742 scores 769 SPECrate®2017_int_peak (701 SPECrate®2017_int_base) http://spec.org/cpu2017/results/res2019q4/cpu2017-20191125-20001. http://spec.org/cpu2017/results/res2019q4/cpu2017-20190429-12779. https://spec.org/cpu2017/results/res2019q2/cpu2017-int_peak. (364 SPECrate2017_int_base) https://spec.org/cpu2017/results/res2019q2/cpu2017-int_peak. (364 SPECrate2017_int_base) https://spec.org/cpu2017/results/res2019q2/cpu2017-int_peak. (364 SPECrate2017_int_base) https://spec.org/cpu2017/results/res2019q2/cpu2017-20190429-12779. https://spec.org/cpu2017/results/res2019q2/cpu2017-20190429-12779. https://spec.org/cpu2017/results/res2019q2/cpu2017-20190429-12779. https://spec.org/cpu2017/results/res2019q2/cpu2017-20190429. https://spec.org/cpu2017/results/res2019q2/cpu2017-20190429. https://spec.org/cpu2017/results/res2019q2/cpu2017/results/res2019q2/cpu2017-20190429. https://spec.org/cpu2017/results/res2019q2/cpu2017/results/res2019q2/cpu2017/results/res2019q2/cpu2017/results/res2019q2/cpu2017/results/res2019q2/cpu2017/results/res2019q2/cpu2017/res2019q2/cpu2017/res2019q2/cpu201
- **5.** Based on standard calculation method for determining FLOPS. ROM-04
- 6. Based on June 8, 2018 AMD internal testing of same-architecture product ported from 14 to 7 nm technology with similar implementation flow/methodology, using performance from SGEMM. EPYC-07

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